QUARTZ CRYSTAL OSCILLATORS

Q: Introduction to Abracon Programmable Oscillators:

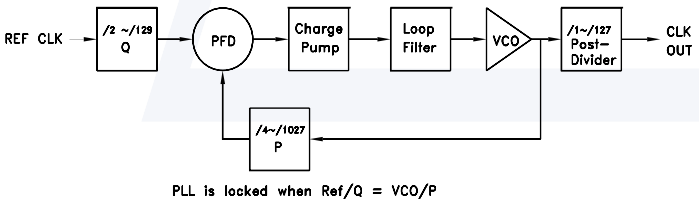
A: Abracon offers quick-turn programmable oscillators in four different package styles; the ceramic package 7.0 x 5.0 x 1.6 mm, plastic molded package similar to Epson SG-8002, and the 14 pin and 8 pin dip packages. The single PLL architecture with EPROM programmable generates a custom frequency derived from an internal crystal between 10MHz to 25MHz. The main advantages of the programmable oscillators are:

- Easy customization and fast turnaround.
- Wide frequency ranges 1MHz to 133MHz.
- Programming accuracy > 6 digits.
- Output control Synchronous or Asynchronous.
- Output levels CMOS or TTL.
- Fast rise and fall times.
- Fast programming time < 5 seconds per unit.
- Low skew, low jitter, high accuracy outputs.
- Enables design flexibility and easy of use.
- Powerdown and output enable options available.
- Configurable 5V or 3.3VDC operation in seconds.
- Reprogrammable for quick design changes (applied to blank only).
- Extended temperature -40°C to +85°C with good frequency vs. temperature characteristics.

Q: What is PLL technology?

A: A PLL allows a frequency to be generated from any other frequency, where:

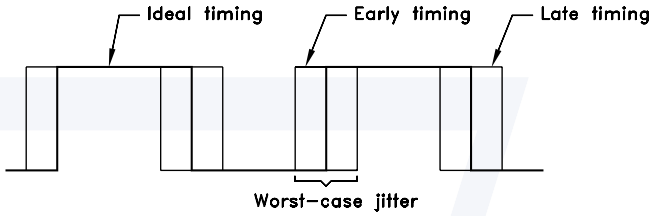
$$\text{CLK OUT} = \frac{\text{REF. CLK} * P/Q}{\text{Post-Divider}}$$



Q: What is jitter?

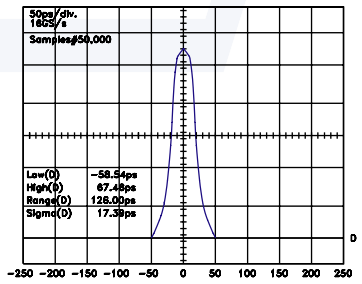
A: Jitter is the uncertainty or short-term variations of a digital waveform timing from their ideal positions in time.

The waveform transition could be too early or too late compared to the ideal waveform timing.



Q: How to measure jitter?

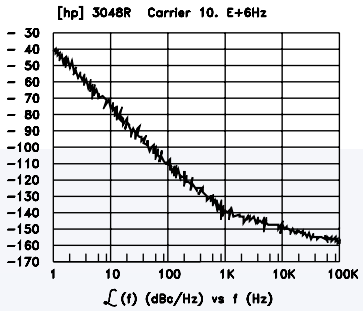
A: We use LeCroy digitizing oscilloscope with jitter timing software for jitter measurement and analysis. The scope must have the bandwidth at least five times the frequency of the waveform since the waveform jitter is measured as each rising cycle crosses the threshold voltage. The larger number of continuous cycles the more accurate is the jitter distribution. Jitter is measured in cycle-to-cycle



(or absolute jitter) or one sigma jitter (rms.) using the histogram analysis. Unit of jitter is ps.

Q: Can phase noise be improved in designs?

A: Yes. Crystal oscillators can be designed to minimize their phase noise characteristics. Special applications such as wireless require best phase noise both at far-end and close-end. Crystal parameters and mounting methods directly affect close-end phase noise 300Hz offset from carrier. The oscillator front-end and output buffer



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Q: Why the Overall frequency stability is specified in crystal oscillators but not in crystals?

A: The crystal oscillator is typically used as a master clock for the microprocessor and its parameters are not affected by the internal characteristics of the microprocessor such as variation in load capacitance and other variables that could affect the change in frequency at room and over temperature. The over all frequency stability in crystal oscillators is typically ±100ppm max. and includes frequency calibration at 25°C, over temperature, frequency changes due to load, supply, aging, vibration, and shock.

Q: What is the start-up time?

A: Start-up time is the delay time between the oscillation starts from noise until it reaches its full output amplitude when power is applied. The supply voltage must be applied with a defined rate or rise. The start-up time varies from microseconds to milliseconds depending on frequency, ASIC speed and logic. Please see figure 1.

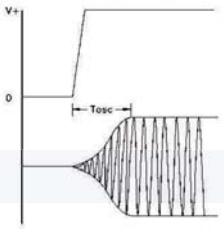


Figure 1

Q: What is Tristate Enable/Disable mode?

A: When the voltage at the control pin is set to a logic low "0",the out put is in Tri-state mode that is High Impedance. The disabled current is usually lower than its normal operating current but not completely cut-off as it was seen in the Stand-by mode, where the oscillation is shut down completely.There is an internal pull-up resistor between control pin and supply (typically 100kΩ), therefore the control pin can be left open (floating) if unused.

Q: What is jitter and how to specify its maximum value?

A: Jitter is noise caused by many sources in crystal oscillators. Major sources of noise are:

- Power supply noise.
- Integer multiples of the signal source frequency (harmonics).
- Load and termination conditions.
- Amplifier noise.
- Circuit configuration (PLLs, Multiplier, Overtone, etc.)

The following methods can be used to suppress the noise conditions in the above sources:

- Make sure that the power supply noise is filtered by using by pass capacitors, chip beads, or RC filters.
- If jitter is critical in some applications, especially for high- fre quencies noise, use low harmonics outputs or sine output.
- Make sure that load and termination conditions are optimized to avoid reflected power back to its output.
- Typically, PLLs, Multiplier or Programmable designs produce higher jitter than the conventional fundamental design.

It is very important to understand the jitter requirements from the application to specify the right specification for crystal oscillators.

We can classify two types of jitters:

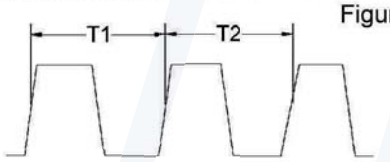
- Cycle to cycle jitter
- Period jitter.

CYCLE TO CYCLE JITTER

The Cycle to cycle jitter is the maximum difference in time between several measured periods. Usually a minimum of ten (10) cycles is used where T1 to T10 were recorded . See fig. 2.

Figure 2

Jitter = Maximum Delta (Ts)



PERIOD JITTER.

The period jitter is the maximum change of a clock edge. It is usually expressed as peak-to-peak jitter and can be converted to rms value by multiplying to (0.5) x (0.707). The period jitter can only be measured at each cycle but not multiple cycles. See figure 3.

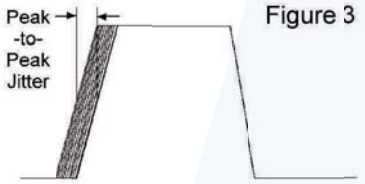


Figure 3

Typical jitter recorded in Abracon oscillators varies from 20ps to 60ps rms.

Q: What is phase noise and how to measure it?

A: Phase noise is the expression of noise in the frequency domain. It is a measure of the short-term frequency fluctuations of the oscillator. It is usually specified as the single sideband power density in a 1Hz bandwidth at a specified offset frequency from the carrier.

In order to measure phase noise, it is necessary to pair a similar device-under-test with one unit set a VCXO and other set a fixed XO. Please see block diagram in figure 4. Typical phase noise in Abracon VCXO and oscillators:

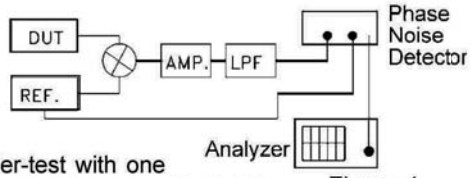


Figure 4

OFFSET FREQUENCY (Hz)	PHASE NOISE (dBc/Hz)
10	-70
100	-110
1,000	-125
10,000	-150
100,000	-160

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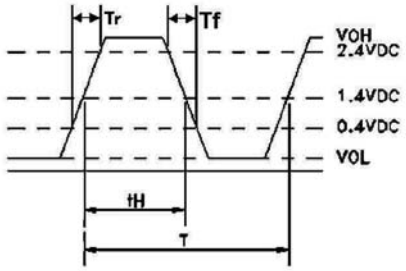
CMOS RISE AND FALL TIMES

The rise and fall time on the CMOS technology depends on its speed (CMOS, HCMOS, ACMOS, BICMOS), the supply voltage, the load capacitance, and the load configuration. Typical rise and fall time for CMOS 4000 series is 30ns, HCMOS is 6ns, and for ACMOS (HCMOS, TTL compatible) is 3 ns max.

Typical rise and fall time is measured between 10% to 90% of its waveform level.



OUTPUT WAVEFORM

Figure 1

ACMOS OUTPUT TERMINATION TECHNIQUES

Due to the fast transition time of the ACMOS (HCMOS/TTL compatible) device, proper termination techniques must be used when testing or measuring electrical performance characteristics.

Termination is usually used to solve the problem of voltage reflection, which essential cause steps in clock waveforms as well as overshoot and undershoot. Such effect could result in false clocking of data, as well as higher EMI and system noise.

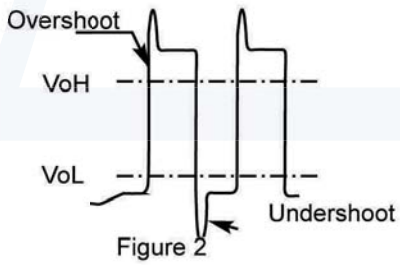


Figure 2

Termination is required also because of the length of the trace on the PC board and its load configuration.

There are three general methods of terminating a clock trace, which is a process of matching the output impedance of the device with the line impedance:

1) Series termination;
2) Pull-up/Pull-down termination;
3) Parallel-AC termination

METHOD 1:

Series termination (Fig. 3)

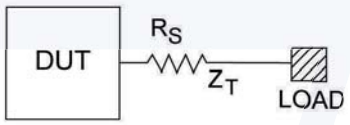


Figure 3

$Rs \geq Z_T - Ro$

In series termination, a damping resistor is placed close to the source of the clock signal. Value of Rs must satisfy the following requirement:

METHOD 2:

Pull-Up / Pull-Down Resistors (Fig. 4)

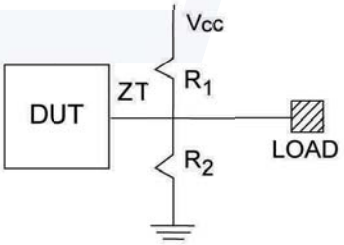


Figure 4

In pull-up/pull-down termination, the Thevenin's equivalent of the combination is equal to the characteristics impedance of the trace. This is probably the cleanest, and results in no reflections, as well as EMI.

$$R_T \sim Z_T$$

METHOD 3:

Parallel AC Termination (Fig. 5)

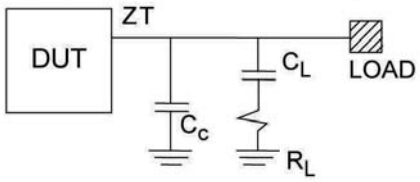


Figure 5

In parallel AC termination, a R-C combination is placed at the load. The value of the capacitor must be chosen carefully, usually smaller than the 50pF. This termination is not recommended because it will degrade the rise and fall time of the clock, although it draws no DC current.

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