CERAMIC SMD CRYSTAL CLOCK OSCILLATOR

APV SERIES

Pb RoHS Compliant

5.0 x 7.0 x 1.8mm

FEATURES:

- Low Phase Jitter 0.7ps max
- CMOS, PECL or LVDS Output

APPLICATIONS:

- SONET, Fiber Channel, SERDES
  HDTV, OBSAI, CPRI, PCI Express, 1394

STANDARD SPECIFICATIONS:

PARAMETERS		
ABRACON P/N:	APV Series	
Frequency range:	38MHz to 640MHz	
Operating temperature:	0° C to + 70° C (see options)	
Storage temperature:	- 55° C to + 125° C	
Overall frequency stability:	± 50 ppm max. (see options)	
Supply voltage (Vdd):	3.3 V or 2.5 V ± 10% (See options)	
Phase Jitter RMS (12KHz - 20MHz)	0.5ps typ, 0.7ps max.	
Period Jitter (peak to peak):	20ps Typ., 30ps max up to 320MHz, 50ps Typ., 70ps max 321MHz to 640MHz	
Tristate Function:	CMOS output	**"1" (V_{IH} ³ 0.7* Vdd) or open: Oscillation** **"0" (V_{IL} < 0.3* V_{dd}): No oscillation/Hi Z**
	PECL output (See TriState Pin Operation table)	**P Option (Standard PECL OE)** **"0" (V_{IL} < 0.3* V_{dd}): or Open: Oscillation** **"1" (V_{IH} < 0.7* Vdd): No oscillation/Hi Z** **P1 Option** **"1" (V_{IH} < 0.7* Vdd) or open: Oscillation** **"0" (V_{IL} < 0.3* V_{dd}): No oscillation/Hi Z**
	LVDS output	**"1" (V_{IH} < 0.7* Vdd) or open: Oscillation** **"0" (V_{IL} < 0.3* V_{dd}): No oscillation/Hi Z**

PECL:	Supply current (I_{DD}): **65mA max (for 38MHz<Fo≤320MHz), 90mA max (320MHz<Fo<640MHz)** Output Logic High: **V_{dd}-1.025V min, V_{dd}-0.880V max.** Output Logic Low: **V_{dd}-1.810V min. V_{dd}-1.620V max.** Symmetry (Duty Cycle): **45% min, 50% typ, 55% max,** Rise time: **0.6ns typ,1.5ns max** Fall time: **0.6ns typ, 1.5ns max**
LVDS	Supply current (I_{DD}): **45mA max (for 38MHz<Fo≤320MHz),70mA max (320MHz<Fo<640MHz)** Output Clock Duty Cycle @ 1.25V: **45% min, 50% typical, 55% max** Output Differential Voltage (V_{OD}): **247mV min, 355mV typical, 454mV max** VDD Magnitude Change (ΔV_{OD}): **-50mV min, 50mV max** Output High Voltage : **V_{OH} = 1.4V typical, 1.6V max.** Output Low Voltage: **V_{OL} = 0.9V min, 1.1V typical** Offset Voltage [R_L = 100Ω] : V_{OS} **= 1.125V min, 1.2V typical, 1.375V max** Offset Magnitude Change [R_L = 100Ω] : **ΔV_{OS} = 0mV min, 3mV typical, 25mV max** Power-off Leakage (I_{OXD}) [Vout=VDD or GND, VDD=0V] = **±1µA typical, ±10µA max.** Differential Clock Rise Time ($_r$) [R_L=100Ω, CL=10pF]: **0.2ns min, 0.7ns typical, 1.0ns,max** Differential Clock Fall Time ($_f$) [R_L=100Ω, CL=10pF]: **0.2ns min, 0.7ns typical, 1.0ns max**
CMOS:	Supply current (I_{DD}): **55mA max (38MHz<Fo<320MHz)** Symmetry (Duty Cycle): **45% min, 50% typ, 55% max,** Rise/Fall time: **(0.3V ~ 3.0V with 15 pF load) 0.7ns Typical** **(20%-80% with 50Ω Load) 0.3ns Typical**

5.0 x 7.0 x 1.8mm

TRI-STATE PIN OPERATION:

OUTPUT TYPE OPTION		PIN 2 logic level*	Output State (Tri-state)
P	PECL	0 (Default)	Enabled
		1	Tri-state
P1	PECL1	1	Enabled
		0	Tri-state
V	LVDS	0	Tri-state
		1(Default)	Enabled
C	CMOS	0	Tri-state
		1(Default)	Enabled

*Connect to VDD for logic level "1", connect to ground for logic level "0".

OPTIONS AND PART IDENTIFICATION

(Left blank if standard)

APV☐ - ☐MHz - ☐-☐-☐-☐

Supply Voltage
Blank*: 3.3V
1: 2.5V

Frequency in MHz
e.g. 24.576MHz 14.31818MHz 26.000MHz

Operating Temp.
Blank: 0°C ~ +70°C
E: -20°C ~ +70°C
L: -40°C ~ +85°C

Frequency Stability
Blank: ± 50 ppm
R: ± 25ppm
S: ± 20ppm

* -20ºC~70ºC and 0ºC~70ºC only.

Output
P: PECL
P1: PECL1
V: LVDS
C: CMOS

Packaging
Blank: Bulk
T: Tape & Reel (1,000pcs/reel)

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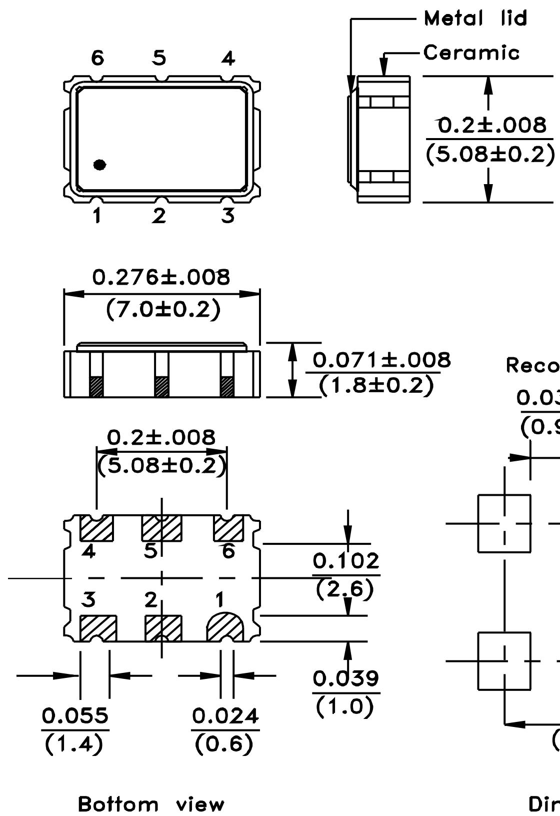
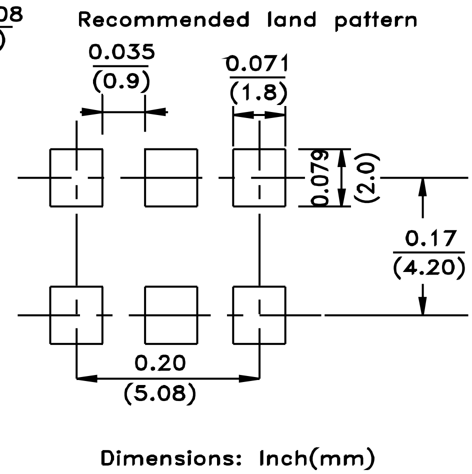
OUTLINE DIMENSIONS: (Effective Date: 12/28/2009)

PECLand LVDS

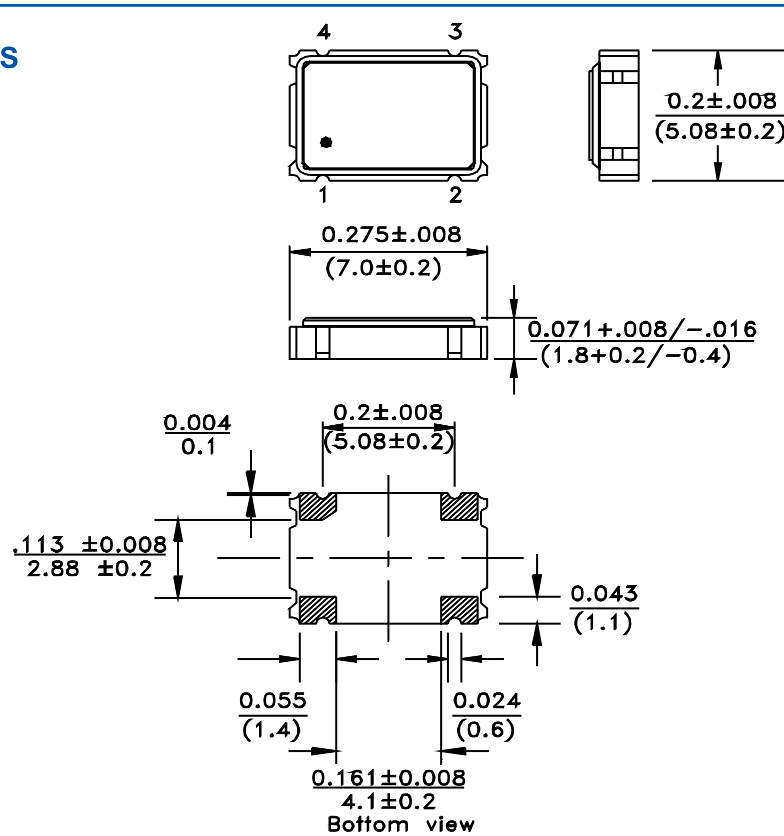


PIN #	Function
1	Tri-state
2	NC
3	GND
4	Q
*5	$\overline{Q}$
6	V_{DD}

*Complimentary PECL/LVDS



CMOS

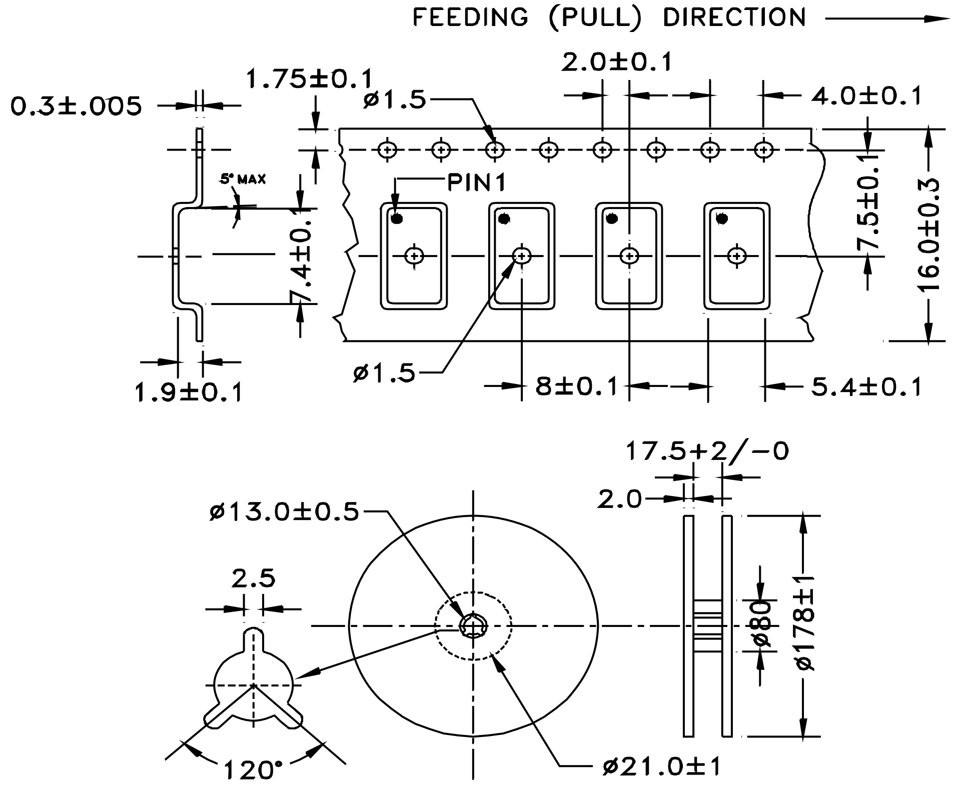


PIN #	Function
1	Tri-state
2	Ground/Case
3	Output
4	Vdd

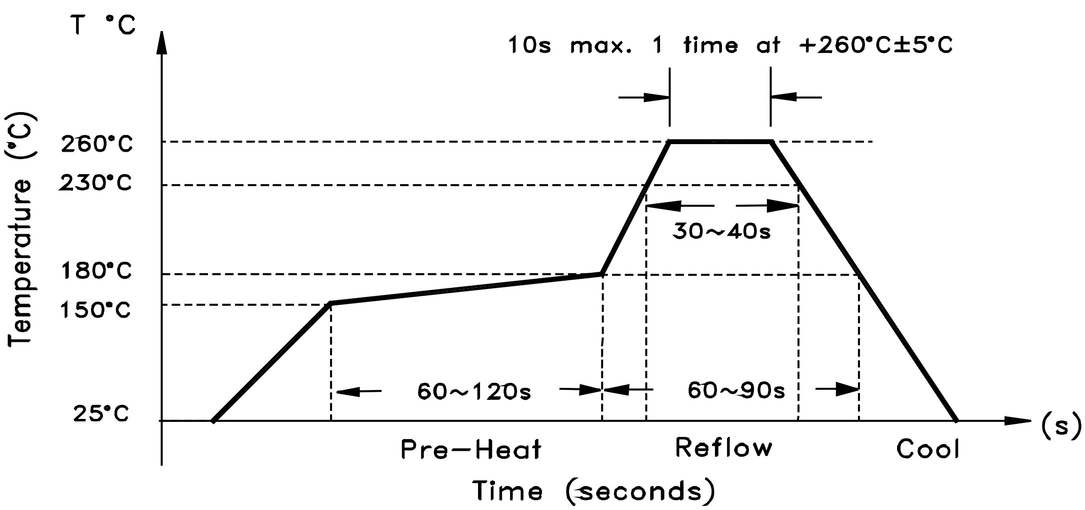
Dimensions: inches (mm)

TAPE AND REEL: T= tape and reel (1,000pcs/reel)

Dimension : mm



REFLOW PROFILE:



NOTE: Abracon manufactured products are intended for general commercial and industrial use. For applications requiring high reliability and/or presenting extreme operating environment, written consent & authorization from Abracon is required.