

# CERAMIC SMD CRYSTAL CLOCK OSCILLATOR WITH VOLTAGE CONTROL



5.0 x 7.0 x 1.8mm

ABVFM SERIES

: PRELIMINARY

## FEATURES:

- Based on a proprietary analog multiplier
- Tri-State Output
- Ultra low Phase Jitter
- 155.52MHz, 311.04MHz, 622.08MHz applications
- 2.5V to 3.3V +/- 10% operation
- Ceramic SMD, low profile package

## APPLICATIONS:

- xDSL, Cable Modems
- Customer Premise Equipment (CPE)
- ATM, SONET, SDH, STB
- LAN / WAN Data Communications Equip.

## STANDARD SPECIFICATIONS:

PARAMETERS	
Frequency Range	60 MHz to 320 MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	- 55°C to + 125°C
Overall Frequency Stability	± 100 ppm max. (see options)
Supply Voltage (Vdd)	2.5V - 3.3 Vdc ± 10%
Jitter (12KHz - 20MHz)	RMS phase jitter < 0.6pS period jitter < 20pS peak to peak
Low Phase Noise	-130 dBc/Hz @ 1kHz Offset from 212.5MHz -140 dBc/Hz @ 10kHz Offset from 212.5MHz -145 dBc/Hz @ 100kHz Offset from 212.5MHz
Aging (PPM/year)	TBD Per Crystal
Pullability	+/- 50ppm
PECL	
Supply Current (I <sub>DD</sub> )[Fout = 212.50MHz]	58mA min, 65mA typical, 75mA max.
Output Clock Duty Cycle @ V <sub>DD</sub> -1.3V	45% min, 50% typical, 55% max.
Output High Voltage	V <sub>OH</sub> = VDD-2V (VDD-1.025V min)
Output Low Voltage	V <sub>OL</sub> = VDD-2V (VDD-1.620V max)
Clock Rise time (t <sub>r</sub> ) @ 20/80%	0.7ns max, 0.4ns typical
Clock Fall time (t <sub>f</sub> ) @ 80/20%	0.7ns max, 0.4ns typical
CMOS	
Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]	1.6ns max, 1.2ns typical
Output Clock Duty Cycle [Measured @ 50% VDD]	45% min, 50% typical, 55% max
LVDS	
Supply Current (I <sub>DD</sub> ) [Fout = 212.50MHz]	60mA max, 55mA typical.
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V <sub>OD</sub> )	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV <sub>OD</sub> )	-50mV min, 50mV max
Output High Voltage	V <sub>OH</sub> = 1.6V max, 1.4V typical
Output Low Voltage	V <sub>OL</sub> = 0.9V min, 1.1V typical
Offset Voltage [R <sub>L</sub> = 100Ω]	V <sub>OS</sub> = 1.125V min, 1.1V typical, 1.375V max
Offset Magnitude Voltage[R <sub>L</sub> = 100Ω]	ΔV <sub>OS</sub> = 0mV min, 3mV typical, 25mV max
Power-off Leakage (I <sub>OxD</sub> ) [Vout=VDD or GND, VDD=0V]	±10μA max, ±1μA typical
Differential Clock Rise Time (t <sub>r</sub> ) [R <sub>L</sub> =100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max
Differential Clock Fall Time (t <sub>f</sub> ) [R <sub>L</sub> =100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max

